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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,806	TAKEUCHI, TIMOTHY M.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,297,549 to Hiyoshi in view of US Patent No. 5,720,342 to Owens et al., and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 7, Hiyoshi (figures 2A-F) teaches an apparatus comprising:

a package substrate having top (331) and bottom (332) buildup layers disposed on a ceramic substrate core (31), wherein a portion of the substrate core is exposed at a top surface of the package substrate for attachment of a heat spreader (32, 39, 38).

Hiyoshi teaches a ceramic substrate core (31). Hiyoshi differs form the claimed invention by not showing a thermally conductive substrate core. The thermally conductive ceramic substrate is known in the art as shown for example by Owens et al. (column 4, lines 37-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select thermally conductive ceramic substrate, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Hiyoshi and Owens et al. differ from the claimed invention by not showing a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the package substrate. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8) and vias (19) formed therein interconnecting top (20) and bottom (24) conductive traces of the package substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Hiyoshi and Owens et al. because it provides connection between the chip and external device. The combined device shows a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the package substrate.

Regarding claim 8, Hiyoshi teaches the exposed portion of the substrate core (31) extends around the perimeter of the top surface buildup layer (331) (see figure 2A).

Regarding claim 9, Hiyoshi, Owens and Ommen et al. differ in not showing the substrate core is made of metal. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate core is made of metal because it dissipates heat from the chip.

3. Claims 10-15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,118,177 to Lischner et al. in view of US Patent No. 6,297,549 to Hiyoshi, and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 10, Lischner et al. (figure 1) teach an apparatus comprising:

an integrated circuit (130) having a top surface and a backside surface, the integrated circuit (130) mounted to the package substrate (120) with the top surface of the integrated circuit (130) facing the package substrate (120); and

a heat spreader (140) mounted to the substrate core (120), a bottom surface of the heat spreader (140) thermally coupled to the backside surface of the integrated circuit (130).

Lischner et al. differ from the claimed invention by not showing a package substrate having first portions and second portion, and a buildup layer being disposed on only the first portion of the substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) including a thermally conductive substrate, having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Lischner et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows a package substrate including a thermally conductive substrate core, having first portion and second portion, and a buildup layer being disposed on only the first portion of the substrate core; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

Lischner et al. and Hiyoshi further differ from the claimed invention by not showing a package substrate including a plurality of conductive traces and vias formed therein

interconnecting top and bottom surfaces of the package substrate. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8) and vias (19) formed therein interconnecting top (20) and bottom (24) conductive traces of the package substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Lischner et al. and Hiyoshi because it provides connection between the chip and external device. The combined device shows a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the buildup layer.

Regarding claim 11, Lischner et al. teach the heat spreader (140) is thermally coupled to a perimeter portion of the substrate core (120).

Regarding claim 12, Lischner et al. teach the heat spreader (140) is soldered (143) to the substrate core (120).

Regarding claim 13, Lischner et al. teach the heat spreader (140) is made of metal (column 2, lines 64-66).

Regarding claim 14, Lischner et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing the substrate core is made of metal. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate core is made of metal because it dissipates from the chip.

Regarding claim 15, Lischner et al. teach a thermal interface material (142) disposed between the backside surface of the integrated circuit (130) and the bottom surface of the heat spreader (140) (column 2, lines 45-48).

Regarding claim 18, Lischner et al. teach the integrated circuit (130) is mechanically and electrically coupled to the package substrate (120) by a plurality of solder bump interconnections (134).

Regarding claim 19, Lischner et al. teach a printed circuit board (150), wherein the package substrate (120) is mounted on the printed circuit board (150).

Regarding claim 20, Lischner et al. teach the package substrate (120) is mechanically and electrically coupled to the printed circuit board (150) by a plurality of solder bump interconnections (152).

4. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. and Hiyoshi in view of Ommen et al., and further in view of US Patent No. 6,229,204 to Hembree.

The disclosures of Lischner et al., Hiyoshi and Ommen et al. are discussed as applied to claims 10-15, 18, 19 and 20 above.

Regarding claim 16, Lischner et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing a heat sink attached to a top surface of the heat spreader. However, Hembree teaches a heat sink (28) attached to a top surface of the heat spreader (30) (see figures 5 and 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a heat sink of Hembree into the device taught by Lischner

et al., Hiyoshi and Ommen et al. since it is desirable to enhance heat dissipation. The combined device shows a heat sink attached to a top surface of the heat spreader.

Regarding claim 17, Lischner et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing a fan attached to the heat sink. However, Hembree teaches a fan attached to the heat sink (column 4, lines 13-14). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a fan of Hembree into the device taught by Lischner et al., Hiyoshi and Ommen et al. since it is desirable to increase heat dissipation. The combined device shows a fan attached to the heat sink.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,561,011 to Kohara et al. in view of US Patent No. 6,297,549 to Hiyoshi, and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 21, Kohara et al. (figure 5) teach an apparatus comprising: at least two integrated circuits (6) having top surfaces and backside surfaces, the integrated circuits (6) mounted on a first surface of the package substrate (7) with the top surfaces of the integrated circuits (6) facing the package substrate (7); and a heat spreader (16) thermally coupled to an exposed portion of the substrate core (7), wherein a bottom surface of the heat spreader (16) is thermally connected to the backside surfaces of the integrated circuits (6).

Kohara et al. differ from the claimed invention by not showing a package substrate having top and bottom surface buildup layers disposed on a thermally conductive substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having

layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a package substrate having top and bottom surface buildup layers of Hiyoshi into the device taught Kohara et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows at least two integrated circuit having a top surface and a backside surface, the integrated circuits mounted to the package substrate with the top surface of the integrated circuits facing the package substrate; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

Kohara et al. and Hiyoshi differ from the claimed invention by not showing a package substrate including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the package substrate. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8) and vias (19) formed therein interconnecting top (20) and bottom (24) conductive traces of the package substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Lischner et al. and Hiyoshi because it provides connection between the chip and external device. The combined device shows a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the buildup layer.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara et al. and Hiyoshi in view of Ommen et al., and further in view of US Patent No. 6,215,670 to Khandros.

Regarding claim 22, the disclosures of Kohara et al., Hiyoshi and Ommen et al. are discussed as applied to claim 21 above.

Kohara et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing one or more capacitors mounted on a top surface of the package substrate. However, Khandros teaches one or more capacitors mounted on a top surface of the package substrate (column 12, lines 40-43; lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the capacitors of Khandros into the device taught by Kohara et al., Hiyoshi and Ommen et al., since it is desirable to improve electrical performance of semiconductor devices operating at high frequencies.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara et al. and Hiyoshi in view of Ommen et al., and further in view of US Patent No. 6,118,177 to Lischner et al.

Regarding claim 23, the disclosures of Kohara et al., Hiyoshi and Ommen et al. are discussed as applied to claim 21 above.

Kohara et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing the heat spreader is soldered to the substrate core. However, Lischner et al. (figure 1) teach the heat spreader (140) is soldered (143) to the substrate core (120). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate

the teaching of Lischner et al. into the device taught by Kohara et al., Hiyoshi and Ommen et al. because it is securely hold the heat spreader in place.

8. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. in view of Hiyoshi, and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 24, Lischner et al. (figure 1) teach an apparatus comprising:

an integrated circuit (130) having a top surface and a backside surface, the integrated circuit (130) mounted to the package substrate (120) with the top surface of the integrated circuit (130) facing the package substrate (120); and

a heat spreader (140) mounted to the substrate core (120), a bottom surface of the heat spreader (140) thermally coupled to the backside surface of the integrated circuit (130).

Lischner et al. differ from the claimed invention by not showing a package substrate having first portions and second portion, and a buildup layer being disposed on only the first portion of the substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) including a thermally conductive substrate, having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Lischner et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows a package substrate including a thermally conductive substrate, having first portion and second portion, and a

buildup layer being disposed on only the first portion of the substrate core; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

Lischner et al. and Hiyoshi further differ from the claimed invention by not showing a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the package substrate. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8) and vias (19) formed therein interconnecting top (20) and bottom (24) conductive traces of the package substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Lischner et al. and Hiyoshi because it provides connection between the chip and external device. The combined device shows a package substrate having top and bottom buildup layers including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the package substrate.

Regarding claim 25, Lischner et al. teach the heat spreader (140) is thermally coupled to a perimeter portion of the substrate core (120).

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. and Hiyoshi in view of Ommen et al., and further in view of US Patent No. 6,229,204 to Hembree.

Regarding claim 26, the disclosures of Lischner et al., Hiyoshi and Ommen et al. are discussed as applied to claims 24-25 above.

Lischner et al., Hiyoshi and Ommen et al. differ from the claimed invention by not showing a heat sink attached to a top surface of the heat spreader. However, Hembree teaches a heat sink (28) attached to a top surface of the heat spreader (30) (see figures 5 and 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a heat sink of Hembree into the device taught by Lischner et al., Hiyoshi and Ommen et al. since it is desirable to enhance heat dissipation. The combined device shows a heat sink attached to a top surface of the heat spreader.

Response to Arguments

10. Applicant's arguments with respect to claims 10-23 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's arguments filed 12/19/03 have been fully considered but they are not persuasive.

It is argued, in page 10 of the remarks, that Hiyoshi, Owens et al. and Ommen et al. do not teach or suggest the claimed invention of claim 7. This argument is not convincing because the combined device (Hiyoshi, Owens et al. and Ommen et al.) shows the claimed invention of claim 7 for the reasons that are discussed above.

It is argued, in page 17 of the remarks, that Lischner et al., Hiyoshi and Ommen et al. do not teach or suggest the claimed invention of claim 24. This argument is not convincing because the combined device (Lischner et al., Hiyoshi and Ommen et al.) shows the claimed invention of claim 24 for the reasons that are discussed above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
March 29, 2004

Primary Examiner
Steven Loke